

APPLICATION FOR UNITED STATES LETTERS PATENT

FOR

BURST TRANSFER REGISTER ARRANGEMENT

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BURST TRANSFER REGISTER ARRANGEMENT

BACKGROUND

[0001] A bus of a computing device may support burst writes wherein multiple writes to contiguous addresses may be performed with a single write to a first address of the contiguous addresses. A burst write to transfer data may take less time to complete than multiple writes to transfer the same data. Similarly, a bus of a computing device may also support burst reads wherein multiple reads from contiguous addresses may be performed with a single read from a first address of the contiguous addresses. A burst read to transfer data may take less time to complete than multiple reads to transfer the same data. Burst writes and bursts reads may therefore improve performance of the computing device.

[0002] Further, a computing device may include several devices to perform certain functions. For example, the computing device may include a graphics card to generate video signals, a network card to interface with a network, and a sound card to generate audio signals. These devices often include registers via which the device may be configured and/or controlled. In particular, the commands and arguments may be written to these registers in order to request the device to execute the command using the supplied arguments. Further, these registers may be read in order to obtain status and output from the command. If writing to and/or reading from these registers may be done in bursts, then the computing device may increase overall performance levels.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] The invention described herein is illustrated by way of example and not by way of limitation in the accompanying figures. For simplicity and clarity of illustration, elements illustrated in the figures are not necessarily drawn to scale. For example, the dimensions of some elements may be exaggerated relative to other elements for clarity. Further, where considered appropriate, reference labels have been repeated among the figures to indicate corresponding or analogous elements.

[0004] FIG. 1 illustrates an embodiment of a computing device with an integrated graphics controller chipset.

[0005] FIG. 2 illustrates an embodiment of a register arrangement to permit a burst write of commands and their arguments which may vary in number.

[0006] FIG. 3 illustrates an embodiment of a method to burst write a command and its arguments and to burst read status and outputs of the command.

DETAILED DESCRIPTION

[0007] The following description describes register arrangement and burst transfer techniques. In the following description, numerous specific details such as logic implementations, opcodes, means to specify operands, resource partitioning/sharing/duplication implementations, types and interrelationships of system components, and logic partitioning/integration choices are set forth in order to provide a more thorough understanding of the present invention. It will be appreciated, however, by one skilled in the art that the invention may be

practiced without such specific details. In other instances, control structures, gate level circuits and full software instruction sequences have not been shown in detail in order not to obscure the invention. Those of ordinary skill in the art, with the included descriptions, will be able to implement appropriate functionality without undue experimentation.

[0008] References in the specification to "one embodiment", "an embodiment", "an example embodiment", etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases are not necessarily referring to the same embodiment. Further, when a particular feature, structure, or characteristic is described in connection with an embodiment, it is submitted that it is within the knowledge of one skilled in the art to effect such feature, structure, or characteristic in connection with other embodiments whether or not explicitly described.

[0009] Embodiments of the invention may be implemented in hardware, firmware, software, or any combination thereof. Embodiments of the invention may also be implemented as instructions stored on a machine-readable medium, which may be read and executed by one or more processors. A machine-readable medium may include any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computing device). For example, a machine-readable medium may include read only memory (ROM); random access memory (RAM); magnetic disk storage media; optical storage

media; flash memory devices; electrical, optical, acoustical or other forms of propagated signals (e.g., carrier waves, infrared signals, digital signals, etc.), and others. Further, firmware, software, routines, instructions may be described herein as performing certain actions. However, it should be appreciated that such descriptions are merely for convenience and that such actions in fact result from computing devices, processors, controllers, or other devices executing the firmware, software, routines, instructions, etc.

[0010] An embodiment of a computing device is shown in FIG. 1. The computing device may comprise one or more processors 100 and a chipset 102. The chipset 102 may include one or more integrated circuit packages or chips that couple the processor 100 to a memory 104. The chipset 102 may further couple the processor 100 to other components 106 such as, for example, BIOS firmware, keyboards, mice, storage devices, network interfaces, etc. via one or more buses.

[0011] The chipset 102 may comprise a memory controller 108 to read from and/or write data to the memory 104 in response to read and write requests of the processor 100 and/or other components of the computing device. The memory 104 may comprise one or more memory devices that provide addressable storage locations from which data may be read and/or to which data may be written. The memory 104 may also comprise one or more different types of memory devices such as, for example, DRAM (Dynamic Random Access Memory) devices, SDRAM (Synchronous DRAM) devices, DDR (Double Data Rate) SDRAM devices, or other volatile and/or non-volatile memory devices. In

one embodiment, the memory 104 may store a graphics driver 110 and an add-in module 112 which the processor 100 may execute in order to control the operation of a graphics controller.

[0012] As depicted, the chipset 102 may comprise an integrated graphics controller 114. In one embodiment, the graphics driver 110 may request the graphics controller 114 to generate an analog display signal suitable for a conventional display monitor 116 such as, for example, a VGA (Video Graphics Array) CRT (cathode ray tube) monitor. Similarly, the graphics driver 110 may request the graphics controller 114 to generate pixel data and provide the generated pixel data to a display codec 118. In one embodiment, the graphics controller 114 may provide the display codec 118 with the pixel data via a DVO (Digital Video Output) port or an SDVO (Serial Digital Video Output) port and associated video interface bus 120.

[0013] Further, the add-in module 112 may control the operation of the display codec 118 and may request information from the display codec 118. In one embodiment, the add-in module 112 may request the graphics controller 114 to write a command and arguments to control registers 122 of the display codec 118 in order to control the operation of the display codec 118 and/or to request information from the display codec 118. The add-in module 112 may further request the graphics controller 114 to read status and/or outputs from the control registers 122 of the display codec 118. In one embodiment, the graphics controller 114 may read from and write to the control registers 122 of the display

codec 118 via a control bus 124 such as, for example, an I2C (Inter Integrated Chip) bus.

[0014] The display codec 118 may receive the pixel data from the graphics controller 114 via the video interface bus 120 and may generate video signals representative of the pixel data that is suitable for other displays 126. In particular, the display codec 118 may comprise core logic 128 to generate television signals such as, for example, SDTV (standard definition television) signals and HDTV (high definition television) signals suitable for a television display. The core logic 128 of the display codec 118 may also generate digital video signals such as, for example, digital video interface signals for flat panel displays or digital CRT signals for digital CRT monitors. Further, in response to a command and its arguments being stored in the control registers 122, the core logic 128 may execute the command in accordance with its arguments and may store status and outputs of the command in the control registers 122.

[0015] In one embodiment, the display codec 118 may be mounted to a motherboard or mainboard (not shown) of the computing device. In another embodiment, the display codec 118 may be mounted to an add-in card such as, for example, an ADD (Advanced Digital Display) card that may be inserted into an AGP port (not shown) of the computing device or an ADD2 (Advanced Digital Display 2) card that may be inserted into a PCI Express port (not shown) of the computing device.

[0016] One possible arrangement of some registers of the control registers 122 of the display codec 118 is shown in FIG. 2. In particular, the depicted

arrangement supports a burst write of a command and its arguments to the appropriate control registers 122 and a burst read of status and outputs of the command from the appropriate control registers 122. However, other arrangements of the control registers 122 are contemplated by the present invention and appended claims. Further, it should be appreciated that the register arrangement of FIG. 2 may also be used by devices and buses other than display codecs and control buses.

[0017] As depicted, the control registers 122 may comprise argument registers 130₁ ... 130_N and a command register 132. The argument registers 130₁ ... 130_N may store arguments of a command and the command register 132 may store a command. As indicated above, writing a command to the command register 132 of the display codec 118 may trigger execution of the command in one embodiment. Accordingly, the graphics controller 114 may write any arguments for the command to the appropriate argument registers 130₁ ... 130_N prior to writing the command to the command register 132.

[0018] In one embodiment, the argument registers 130₁ ... 130_N and the command register 132 are contiguously writable with the argument registers 130₁ ... 130_N arranged in a reverse order followed by the command register 132. In particular, the address of first argument register 130₁ may be greater than the address of the second argument 130₂, the address of the second argument register 130₂ may be greater than the address of the third argument register 130₃, and so on. Further, the address of the command register 132 may be greater than the address of the first argument register 130₁ thus resulting in the

address of the command register 132 coming after the addresses of the argument registers 130₁ ... 130_N.

[0019] As a result of such an arrangement, a single burst write of a command and its X arguments may start from the address of the Xth argument register 130_X and may respectively store the Xth arguments to the first argument in the argument registers 130_X ... 130₁ and a command in the command register 132 regardless of whether the command has 0 arguments, N arguments, or some quantity of arguments between 0 and N. For example, the graphics controller 114 may request the display codec 118 to execute a command having three arguments by issuing a single burst write of the three arguments and the command to the address of the third argument register 130₃ thus resulting in the three arguments registers 130₃, 130₂, 130₁ respectively storing the third argument, second argument, and first argument of the command and the command register 132 storing the command.

[0020] The register arrangement may further comprise a status register 134 and output registers 136₁ ... 136_M. The status (e.g. OK, In Process, Error) of a command may be stored in the status register 134. Further, any outputs of the command may be stored in the output registers 136₁ ... 136_M by placing the first output in the first output register 136₁, the second output in the second output register 136₂ and so on until the last output of the command is stored in the Yth output register 136_Y.

[0021] In one embodiment, the status register 134 and the output registers 136₁ ... 136_M are contiguously readable with the status register 134 followed by

the output registers $136_1 \dots 136_N$. In particular, the address of status register 134 may be less than the address of first output register 136_1 , the address of the first output register 136_1 may be less than the address of the second output register 136_2 , and so on. As a result of such an arrangement, a single burst read may start from the address of the status register 134 and read status from the status register 134 and outputs from the first output register 136_1 to the last output register 136_Y associated with the command regardless of whether the command has 0 outputs, M outputs, or some quantity of outputs between 0 and M . For example, the graphics controller 114 may obtain from the display codec 118 the status and outputs of a command having two outputs by issuing a single burst read that starts from the address of the status register 134 and stops after reading the second output register 136_2 .

[0022] An embodiment of a method to burst write a command and its arguments to a display codec 118 and to burst read status and outputs of the command from the display codec 118 is shown in FIG. 3. In block 200, the processor 100 in response to executing the add-in module 112 may determine an address of the display codec 118 to which a burst write of a command and its arguments may be directed. In one embodiment, the processor may determine an argument count for the command that is indicative of the number of arguments for the command and may select the address of the argument register 130 that corresponds to the argument count. For example, if the command has two arguments, then the processor may select the address of the second argument register 130_2 .

[0023] The add-in module 112 in block 202 may further cause the processor 100 to determine a write length of the burst write and a length of a corresponding burst read. In one embodiment, the write length may represent the number of registers to be written during the write burst. Accordingly, the processor 100 may determine the write length by simply incrementing the argument count by one to account for the command. The processor 100 in response to executing the add-in module 112 may further determine in block 204 a read length for a read burst used to obtain status and outputs of the command. In one embodiment, the read length may represent the number of registers to be read during the read burst. Accordingly, the processor 100 may obtain the read length by determining an output count for the command that is indicative of the number of outputs to be generated by the command and incrementing the output count by one to account for the status of the command.

[0024] In block 206, the add-in module 112 also cause the processor 100 to arrange the command and its arguments for the burst write. In one embodiment, the processor 100 may contiguously store the arguments in memory 104 in a reverse order in which the last argument is stored first and the first argument is stored last. Further, the processor may store the command after the reversed arguments. After arranging the arguments and command, the processor 100 in block 208 may request the graphics controller 114 to burst write the arguments and command to the address determined in block 200 and to burst read the status and outputs of the command from the address associated with the status register 134. To this end, the processor 100 may provide the graphics controller

114 with the address determined in block 200, the address of the status register 134, the write length, and the read length.

[0025] In response to the request, the graphics controller 114 in block 210 may burst write the arguments and command to the display codec 118. In one embodiment, the graphics controller 114 may retrieve the arguments and command from the memory 104 and may start writing from the address determined in block 200 and stopping after writing to the command register 132 as indicated by the write length determined in block 202. During the burst write, the graphics controller 114 may transfer the arguments and command across the control bus 124 to the display codec 118 in the order that the processor 100 arranged the arguments and command in the memory 104.

[0026] In one embodiment, the burst write results in the display codec 118 receiving the arguments in reverse order. In particular, the last received argument corresponds to the first argument of the command, the next to last received argument corresponds to the second argument of the command, etc. with the first received argument corresponding to the last argument of the command. The display codec 118 in block 212 may store the received arguments in the argument registers 130₁ ... 130_x and the received command in the command register 132. In particular, the display codec 118 may store the first received argument in the Xth argument register 130_x per the address determined in block 200, may store the second received argument in the next argument register 130_{x-1}, and so on until the display codec 118 stores the last received argument in the first argument register 130₁. Further, the display codec 118 may

receive the command after the arguments and may store the received command in the command register 132.

[0027] In response to storing the command in the command register 132, the core logic 128 may execute the command in accordance with the arguments stored in the argument registers 130₁ ... 130_X (block 214). Upon completing the command, the core logic 128 in block 216 may store status and outputs of the command in the status register 134 and output registers 136₁ ... 136_Y.

[0028] The graphics controller 114 after waiting a predetermined amount of time after the burst write may burst read the status and outputs from the display codec 118 via the control bus 124 (block 218). In one embodiment, the graphics controller 114 during the burst read may start reading from the status register 134 and continuing reading from the first output registers 136₁ to the Yth output register 136_Y associated with the last output of the command. In particular, the graphics controller 114 may identify the Yth output register 136_M based upon the read length supplied by the processor 100. By first reading the status, the graphics controller 114 may abort the burst read based upon the status before reading all outputs of the command. For example, if the status indicates that the display codec 118 has yet to complete the command, then the graphics controller 114 may abort the burst read before reading all the output registers 136₁ ... 136_Y associated with the command and retry the burst read at a later time when the display codec 118 has likely completed execution of the command.

[0029] Finally, the graphics controller 114 in block 220 in response to receiving the status and outputs from the display codec 118 may return the

status and outputs to the add-in module 112 for further processing and/or analysis.

[0030] Certain features of the invention have been described with reference to example embodiments. However, the description is not intended to be construed in a limiting sense. Various modifications of the example embodiments, as well as other embodiments of the invention, which are apparent to persons skilled in the art to which the invention pertains are deemed to lie within the spirit and scope of the invention.